APPLICATION

FOR

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TITLE: DUAL SENSITIVITY IMAGE SENSOR

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DUAL SENSITIVITY IMAGE SENSOR

This application claims priority from Provisional application no 60/139345, filed 6/15/99.

BACKGROUND

The dynamic range of a typical CMOS image sensor is between 65 and 75dB. The scene dynamic range, however, may extend over more than 5 orders of magnitude. If the scene dynamic range exceeds the sensor dynamic range, then portions of the image may be clipped or distorted in the darkest or brightest areas of the scene.

Techniques for extending dynamic range have included using both non-linear sensors and linear sensors. The non-linear sensors may cause image lag, have a large pixel size, cause inflexible or destructive compression, loss of contrast, increased noise or long integration time. Linear sensors may have excellent contrast and improved noise processing. They may also produce excellent opportunities for post-processing, since the output is typically directly related to the input.

A high dynamic range linear sensor often takes several integrations of the same scene. Each integration has a

different integration time. The varying sensitivity of the different integrations can provide more information about the scene. When each integration is completed, each pixel may be accessed several times to obtain all the information. This necessity to access the pixels may decrease the frame rate of the sensor. A frame memory may also be necessary to store the results of the integration temporarily.

SUMMARY

The present system uses obtains two integrations of the same image, at the same time, using a photoreceptor, and the auxiliary part for the photoreceptor.

An embodiment discloses using a photogate which has an associated floating diffusion used. Both the photogate and the floating diffusion simultaneously acquire information about the image. The photogate may be more efficient and produces a higher sensitivity value than the floating diffusion. In this way, both a high and a low sensitivity version of the image can be obtained. The information may have an increased dynamic range.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects will now be described in detail with reference to the accompanying drawings.

Figure 1A shows the layout of a CMOS image sensor array including the image acquisition part and the signal processing part;

Figure 1B shows a circuit diagram of a single pixel and a single part of the column signal processor; and

Figure 2 shows a diagram illustrating the flow of operation.

DETAILED DESCRIPTION

The present application describes using a photoreceptor of a type that has an associated part that stores charge. The photoreceptor can include a photogate and the associated part can be a floating diffusion that stores charge from the photogate. This can facilitate obtaining two images of the same scene at the same time. The two images have different sensitivities. It is recognized by the present inventors that the photogate pixel actually has two electron collecting areas. The photogate itself collects electrons. The floating diffusion area also collects electrons, but does so at a lower efficiency, as compared with the photogate.

Hence, during the integration period, the photogate area generates a higher sensitivity signal, and the floating diffusion generates a lower sensitivity signal. The lower sensitivity signal may have an integration time which is equal to or less than the integration time of the higher sensitivity signal. The lower sensitivity node is 30 to 40 times less sensitive than the high sensitivity node. This sensitivity, however, can vary depending on the ratio between photogate area and area of the floating diffusion. Different pixels can be designed with different ratios. These can be determined, for example, by trial and error.

Figure 1A shows an overall layout of the sensor chip. A single silicon substrate 99 has integrated therein a photosensor array 100 which includes a plurality of pixel photosensor elements arranged in rows and columns. Each of the pixels, such as 102, preferably has the same structure. The same substrate 99 also includes an image processor part 110, formed of a plurality of circuits 112. Each of the image processor circuits preferably has identical structure. Also integrated on the chip 99 is a controlling element 120, which produces control signals that control the flow of the operation on the chip.

Each of the transistors on the substrate are preferably formed of MOS type circuit elements. The control structure can be CMOS.

Figure 1B shows a detailed schematic of the structure of the pixels 102 and an associated processing circuit 112. The signals described herein are produced by the control circuit 120, which can be a small processor, or can be hardwired logic, which is created using hardware definition language. The system preferably uses a photosensor of a type which has an associated charge storage part. One recognition of the present application is that this associated charge storage part will also integrate charge from incoming light. However, the charge integration may be less efficient than the actual photoreceptor. In this embodiment, the photoreceptor is a photogate 150, which has an associated node 151. The node 151 is maintained separated from a floating diffusion 152. A transfer gate 154 seperates the charge stored in the photogate 150 from the floating diffusion 152. The TX gate is held at a fixed voltage of about 1.2 volts, which is a slightly "ON" state. This forms a barrier to the charge under the photogate, when the photogate is biased high, say at 5 volts. When the photogate is pulsed low, e.g., to 0 volts, the TX gate

forms a channel, allowing the charge to pass to the floating diffusion. The control of the photogate voltage PG is produced by the control circuit 120.

The level of the floating diffusion can be adjusted by the reset transistor 155. The reset signal RXT connects the reset transistor to the voltage V_{AA}, which is a reset voltage. The level on floating diffusion 152 is also buffered by a follower 158, and can be sampled. A row select transistor 160 is actuated by the control circuit 120 to select that specified row of pixels. A plurality of other row select transistors from different rows are connected to the node 162. Only one row is preferably selected at any one time. Each column of pixels is associated with a column signal processor shown as 112. The column signal processor processes the signals described herein. As shown, three sample and hold circuits are provided. A first sample and hold circuit 165 stores the reset level. The SH_RST signal from the control circuit 120 turns on the transistor 166 thus storing the reset level into the capacitor 168. Analogously, the other sample and hold circuit 170 stores the floating diffusion level, and the third sample and hold circuit 175 stores the photogate signal. An arithmetic processor 175 can be

provided to provide any desired combination of these signals.

The low sensitivity signal can correspond to the floating diffusion values subtracted from the reset value. The photogate value can correspond to the photogate sample and hold level, subtracted from the floating diffusion value, and optionally also subtracted from the reset value. Each of the pixels in a specific row receives the same row select signal to the base of the transistor 160 that is associated with each pixel in that row. This turns on all of the transistors in a row at once, thereby selecting the entire row at once. All transistors in all other rows are maintained off. One value from each column is thereby obtained at any time, into a corresponding signal processing unit 112. This allows the system to operate in a so-called column/parallel mode wherein an entire row of pixel outputs are obtained.

The operation occurs as shown in Figure 2. During each cycle, the system is first reset as shown as 250, to a reset level. The reset value is sampled at 255. The reset value is sampled during this time by selecting the row, and actuating the SH_RST signal to provide the reset signal onto the associated capacitor 168. The photogate mode

integration begins at the time of reset shown as 240. The floating diffusion integration begins at time 245, after the sample reset value is detected.

At the end of the integration time, the floating diffusion 152 has integrated charge. This is sampled at time 200, to obtain the value of the FD sample. This value is then actuated into the sample and hold circuit 170. The photogate also includes charge. After sampling the floating diffusion, the transfer gate 154 is actuated by producing the signal TX from the controller. This dumps the charge from the photogate 150 into the floating diffusion and the floating diffusion is again sampled at 210 to obtain the photogate value. This value is then held in the sample and hold 175.

Both the photogate and the floating diffusion integrate during the same time period. At least 80% of the integration time is preferably common. The time of integration of the FD may be slightly less, to accommodate sampling values on the floating diffusion. However, since the time of integration is mostly common, the same scene is imaged.

Although only a few embodiments have been disclosed in detail above, other embodiments are possible. For example,

while the embodiment disclosed above describes using the photogate, it could also be done with other kinds of light sensing devices. An important feature is that two different levels of charge, at two different sensitivities, are sampled into different node at least partly simultaneously.

All such modifications are intended to be encompassed within the following claims.